A Direct Conversion RF Front-End for 2-GHz WCDMA and 5.8-GHz WLAN Applications

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Abstract — **A direct conversion RF front–end for 2.0–GHz WCDMA and 5.8–GHz WLAN applications is described. The measured double-sideband NF, IIP3 and voltage gain are 3.6 dB, –15.1 dBm and 29.5 dB for WCDMA, and 5.2 dB, –17.4 dBm and 26.5 dB for WLAN, respectively. The RF front-end consumes 22.3 mA in WCDMA mode and 23.1 mA in WLAN mode from a 2.7–V supply. The chip is fabricated using a 0.35-μm 45–GHz SiGe BiCMOS process.**

I. Introduction

Recently published RF front-ends and receivers for multi-band operation have usually been implemented using several parallel RF paths [1]–[3]. These front-ends typically combine systems operating below 2.5 GHz, for example WCDMA and GSM. However, due to limited capacity of these systems, frequencies above 2.5 GHz are becoming popular. Hence, systems like IEEE 802.11a (WLAN) should be integrated on same receiver with systems operating below 2.5 GHz.

In this paper, an RF front-end for 2.0-GHz (WCDMA) and 5.8-GHz (WLAN) systems is presented. Because of a wide gap between the operating frequencies, several design aspects must be taken into account when combining the circuits. The highest integration level would be achieved if no parallel blocks were used. However, this approach usually leads to solutions, which are not optimal for all used systems. In the designed RF front-end, both systems share the same mixers but in the LNA parallel signal paths are used. Thus, the mixer must be broadband and the phase shift circuit has to be accurate in both operating frequencies in order to receive signals of both systems.

The selection of the receiver topology is critical and usually direct conversion receiver is considered the best alternative for multi-band receivers because there is no need for several off-chip image-reject and channel-select filters.

II. RF Front-End

The RF front-end uses the direct conversion architecture, which is suitable for integrating multi-band terminals. It has some well-known disadvantages, which have been discussed, for example, in [4]. A block diagram of the designed RF front-end, which includes a baseband buffer for measurements, is shown in Fig. 1. It consists of two single-ended LNAs, wideband I/Q-mixers, 90° phase shift network and LO-buffers. The LO-signal is external and a 90° phase shift is performed either with a divide-by-two circuit or RC-polyphase filter depending on the reception frequency. The mixers have been designed to drive directly the baseband circuit, which in this design is designed for measurement purposes only. To enable separate front-end measurements there are two test outputs connected to the mixer output.

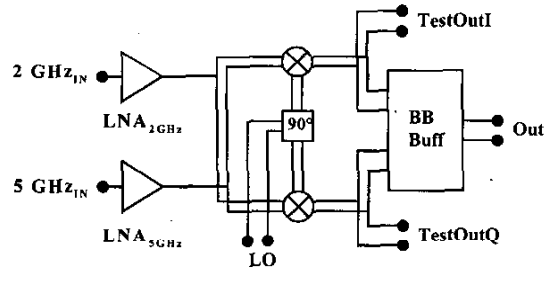

Fig. 1. Block diagram of the RF front-end.

A. LNA

The LNAs are designed to operate either in 2.0-GHz WCDMA system or in 5.8-GHz WLAN system at a time. The LNAs have different RF paths for both operation modes to enable the optimization of the LNA in both modes. For example, if a concurrent LNA was used, the performance of both systems could not be maximized simultaneously which leads to a degraded performance in one mode [5]. In addition, the LNA input stage combination shown in [6] was not chosen to avoid performance degradation due to combined signal paths.

Both LNAs are based on a common-emitter amplifier with inductive emitter-degeneration and a cascode stage. The schematic of the WCDMA mode LNA is shown in the Fig. 2. Both LNAs are similar except the linearization

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circuit (DBF) and the base-emitter capacitance (C_{be}) which are used in WCDMA mode only. Because only one mode is selected to be operational at a time, the power consumption is minimized by shutting the non-operational LNA off. Because both modes have separate RF paths, interference between operational and non-operational systems is minimized.

In both LNAs, the matching of the input transistor is realized with base and emitter inductors and in the case of WCDMA system with a base-emitter capacitance C_{be}. The cascode transistors are important because of the LO leakage problem in direct conversion receivers. From the cascode transistors the signal current is driven into the load resonator. The operating frequencies of the resonators are 2.0 and 5.8 GHz. The resistance in the resonator reduces the Q-value of the resonator thus decreasing the gain and widening operational band. This gives more tolerance against process variations.

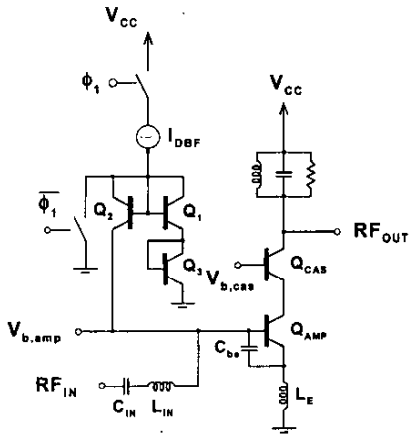

Fig. 2. Schematic of the LNA with a linearization circuit.

In the WCDMA mode LNA, a dual bias feed (DBF) circuit is added to the conventional resistor bias feed. The DBF circuit consists of transistors Q_1-Q_3 and switchable current source I_{DBF}. It provides extra base current into the input transistor when the input signal is strong enough [7]. Higher linearity is achieved at the expense of a higher current consumption and slightly higher NF. With the same collector current of the input transistor, the LNA with a DBF is more linear than a LNA biased only with conventional resistor feed circuit. According to simulations the DBF increases ICP and IIP3 of the LNA by 6.5 dB and 7 dB, respectively. The DBF circuit can be shut off. When it is on, LNAs current consumption increases by 1.3 mA and NF by 0.3 dB.

B. Mixer

The designed downconversion mixer is based on the Gilbert-cell topology. It is double-balanced and uses a cascode transistor (*Qc1,Qc2*) between the input stage (*Qi1,Qi2*) and LO switching transistors (*Q1,Q2,Q3,Q4*). The cascode transistor is added to improve the mixers reverse isolation and on the other hand to relax the interface selection between the mixer and the LNA. The schematic of the mixer is shown in Fig. 3.

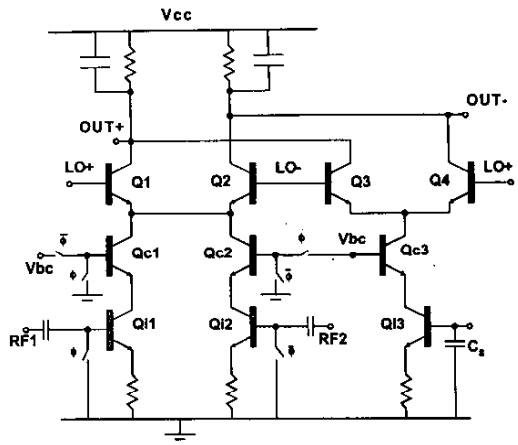

Fig. 3. Schematic of the dual-band downconversion mixer.

A dummy branch was used to prevent the LO amplitude noise to pass to the mixer output. This branch contains a switching pair (*Q3,Q4*), a cascode (*Qc3*) transistor, and an input stage (*Qi3*), which is shunted to the ground with a capacitor (C_s). With this arrangement the LO signal sees the mixer as double-balanced. Emitter degenerated bipolar transistors were used in the input stage because of the high operating frequency. The bandwidth of a MOSFET is insufficient for WLAN and degeneration was used for higher linearity. Furthermore bipolar transistors were used in the switching quad due to their lower 1/f-noise.

Because the mixer is broadband, the same switching core can be used in both systems. The mixer has two separate inputs, one for 2 GHz and one for 5.8 GHz. This is due to the LNA, which has two resonators and therefore two single-ended outputs. For example, if the input *RF1* is used as an active input, then the transistors *Qi2* and *Qc2* are shunted to the ground and transistors *Qi1* and *Qc1* are biased on.

C. Phase shift circuit

The quadrature LO-signals for the I/Q-mixers are generated on the chip from a balanced external LO signal. Because of the performance optimization and the wide

frequency difference between WCDMA and WLAN systems, two different phase shift paths were implemented. The first path consists of a divide-by-two (D-latch) circuit and the other path consists of an RC-polyphase filter and a differential amplifier. The D-latch divider path is used in WCDMA mode, and when receiving in WLAN mode, the RC-polyphase filter path is used. The simplified schematic of the phase shift circuit is presented in Fig. 4.

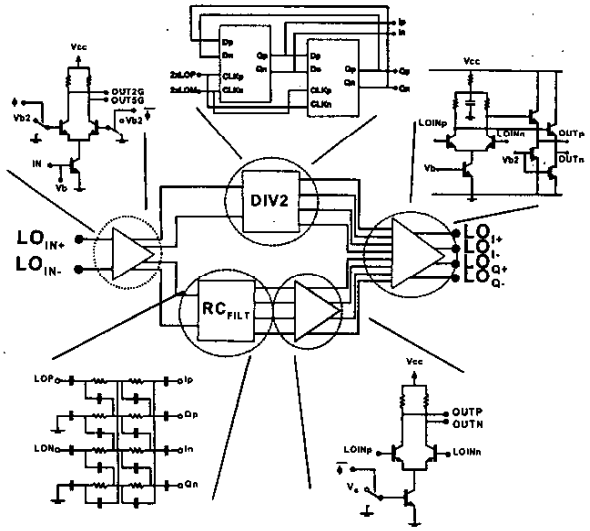

Fig. 4. Schematic of the dual-band phase shift circuit.

At the first stage (Fig. 4), an external LO-signal is steered into the divider or the RC-polyphase filter. The first stage is realized using two common-emitter amplifiers with resistive loads for each branch.

The RC-polyphase filter has two stages. According to simulations, the RC-filter attenuates the LO-signal by 10 dB at 5.8 GHz. The attenuation of the RC-filter is compensated in the differential amplifier stage, which provides 14 dB gain. The amplifier is shut off when using the frequency divider for phase shifting. This reduces current consumption and lowers disturbance that can be generated in the non-active path. The divide-by-two circuit is realized using two cross-clocked D-latches.

If a frequency divider for phase shifting in WLAN mode were to be used, it would require a high maximum operating frequency, which would lead to high current consumption. In addition, an expensive packaging technology would be required to get almost 12 GHz signal into the chip. Additionally, a single phase shift circuit cannot be used in both systems, because too wide operation band would then be required. That would require a several stage RF-polyphase filter, which leads to severe signal losses. To compensate the losses LO-signal should be amplified at least 3 dB per filter stage. Additionally, the noise floor level would be higher. Therefore, a D-latch divider and a RF-polyphase filter combination leads to optimum realization, when considering current consumption, silicon area, and packaging costs.

The last stage of the phase shift circuit is the local buffer and it consists of separate differential pairs followed by an emitter follower, which drives the mixer. The purpose of the local buffer is to choose either 2-GHz or 5.8-GHz signal to be fed to the mixer. In addition the local buffer smoothens the amplitude imbalance between the I- and Q-branches. The local signal amplitude is limited by driving the differential pair into compression. A common-mode resistor is used to shift the common-mode output voltage of the differential pair, and a capacitor is used to filter out the common-mode current. In order to provide sufficient LO-signal amplitude in WLAN mode, an emitter follower had to be included in the LO-buffer. It consumes 4.7 mA in both modes. The emitter follower was not designed to be scalable between different modes, hence it is not optimal for WCDMA. The simulated current consumption of the phase shift circuit is 10.4 mA in WCDMA mode and 11.5 mA in WLAN mode.

III. Experimental results

The chip area including bonding pads is 5.85mm^2. The measurements were performed for chips, which were bonded directly on PCB. In addition, packaged version (VFQFPN44) of the circuit was measured. The measurements were made at the output of the baseband buffer, because the intermodulation distortion at the mixer output have to be amplified. The linearity component of the baseband buffer is high so it doesn't affect the linearity of the whole receiver. In addition, the baseband buffer has a very high CMRR in order to suppress the common-mode distortion components. The NF is measured at the output of the baseband buffer and the NF of the RF-front end is calculated from the NF of the whole receiver. Probably due to the noise from the LO-signal the measured NF is higher than simulated. The measured and simulated RF front-end performance for WCDMA and WLAN is given in Table I. The measured results agreed well with the simulated ones. The measured IIP2 was moderate but it can be improved by resistor tuning presented in [8]. The microphotograph of the receiver is presented in Fig. 5.

TABLE I

SIMULATED AND MEASURED RF FRONT-END PERFORMANCE

Parameter:	Measured: WCDMA	Simulated: WCDMA	Measured: WLAN	Simulated: WLAN
	Bare dice / package	Bare dice	Bare dice / package	Bare dice
Supply voltage	2.7 V	2.7 V	2.7 V	2.7 V
Current cons.	22.3 / 20.3 mA	22.6 mA	23.1 / 23.7 mA	26.9 mA
Voltage gain	29.5 / 28.4 dB	29.7 dB	26.5 / 26.3 dB	26.5 dB
NF (DSB)	3.6 / 3.2 dB	2.5 dB	5.2 / 4.9 dB	4.3 dB
IIP3	–15.1 / –17.5 dBm	–16.3 dBm	–17.4 / –16.3dBm	–18.4 dBm
IIP2	8.0 / 15.0 dBm	–	25.0 / –0.5 dBm	–
ICP	–30.9 / –30.6 dBm	–31.6 dBm	–28.5 / –26.5 dBm	–30.6 dBm
LO at RF input *)	–80.0 / –90.0 dBm	–	–70.6 / – dBm	–
S11	–11.5 / –17.8 dB	–16.3 dB	–17.3 / –11.8dB	–17.4 dB

*) LO–power –10dBm

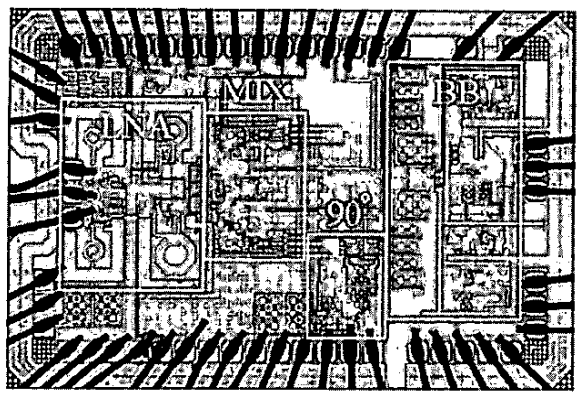

Fig. 5. Microphotograph of the RF front-end.

V. CONCLUSION

A single-chip direct-conversion RF front-end for WCDMA and WLAN applications is presented in this paper. Several design aspects of combining these two systems with a large difference in reception frequencies are discussed. The measured performance, which agreed well with simulations, was achieved using parallel signal paths in the key places and combining the signal at the quadrature mixers.

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